

Building a COTS Benchmark Baseline for Graph Analytics

PageRank acceleration for large graphs with scalable hardware and two-step SpMV

Research Problem

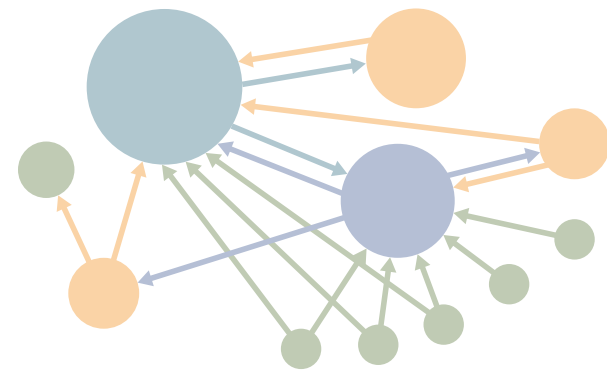
PageRank suffers from poor performance and efficiency due to notorious memory access behavior. More importantly, when graphs become bigger and sparser, PageRank applications are inhibited as most solutions strongly rely on large random access fast memory, which is not scalable.

PageRank vector:

$$x_i = \underbrace{\alpha x_i^T A}_{\text{SpMV}} + (1-\alpha) x_i^T \frac{ee^T}{N}$$

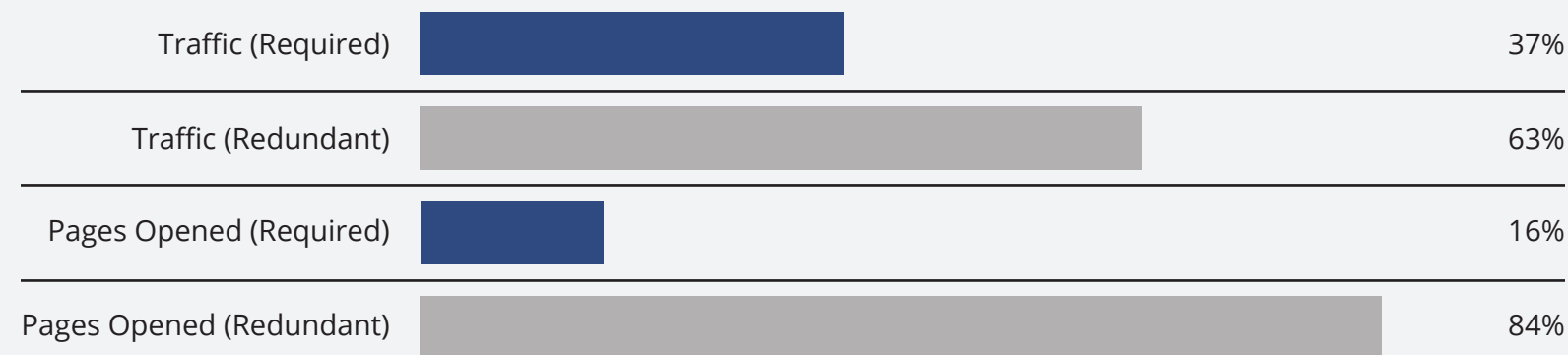
Target Graphs

- Very large (~billion nodes)
- Highly sparse (average degree < 10)
- No exploitable non-zero pattern

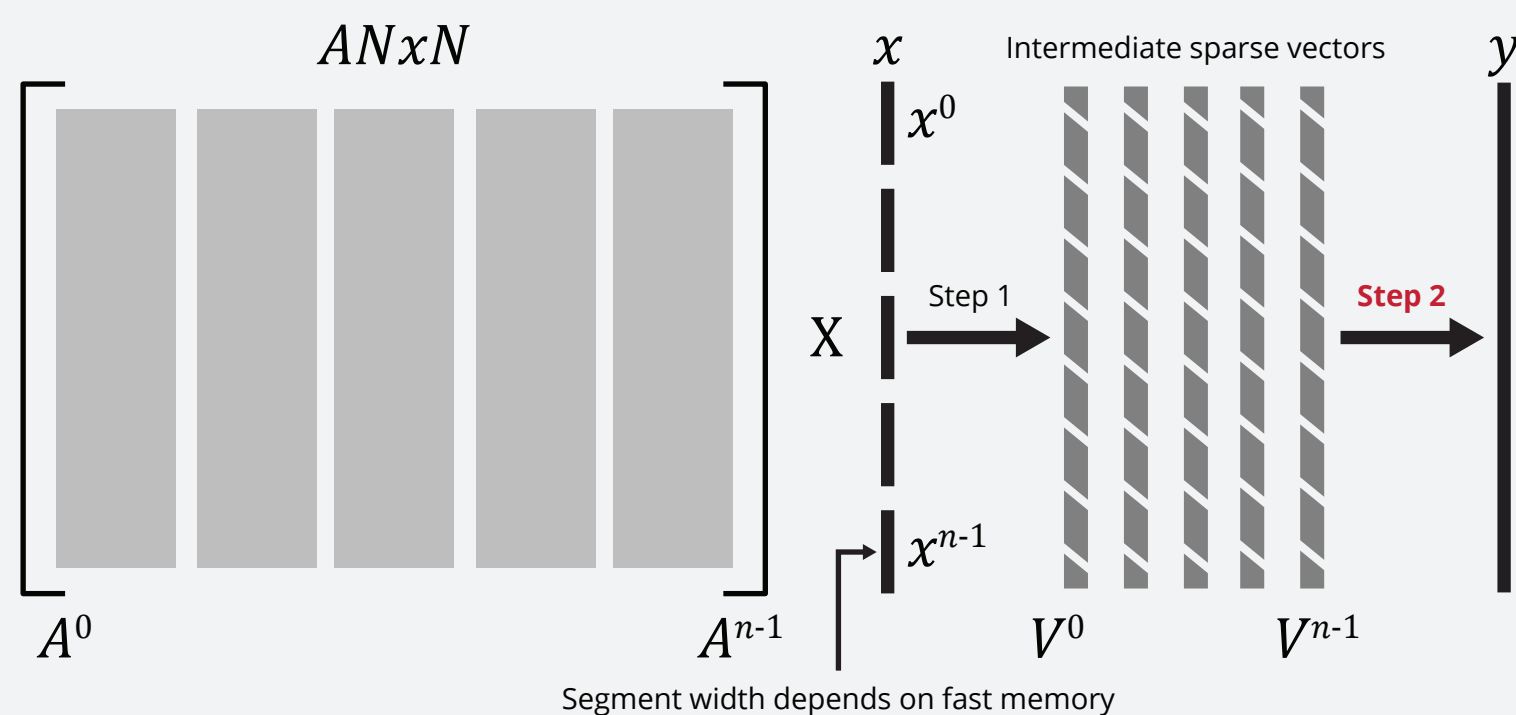


Two-Step SpMV Algorithm

Baseline SpMV: 80M nodes, Avg. degree 3



Two-step algorithm conducts SpMV in two separate steps. It requires blocking of the matrix and the source vector as shown below.

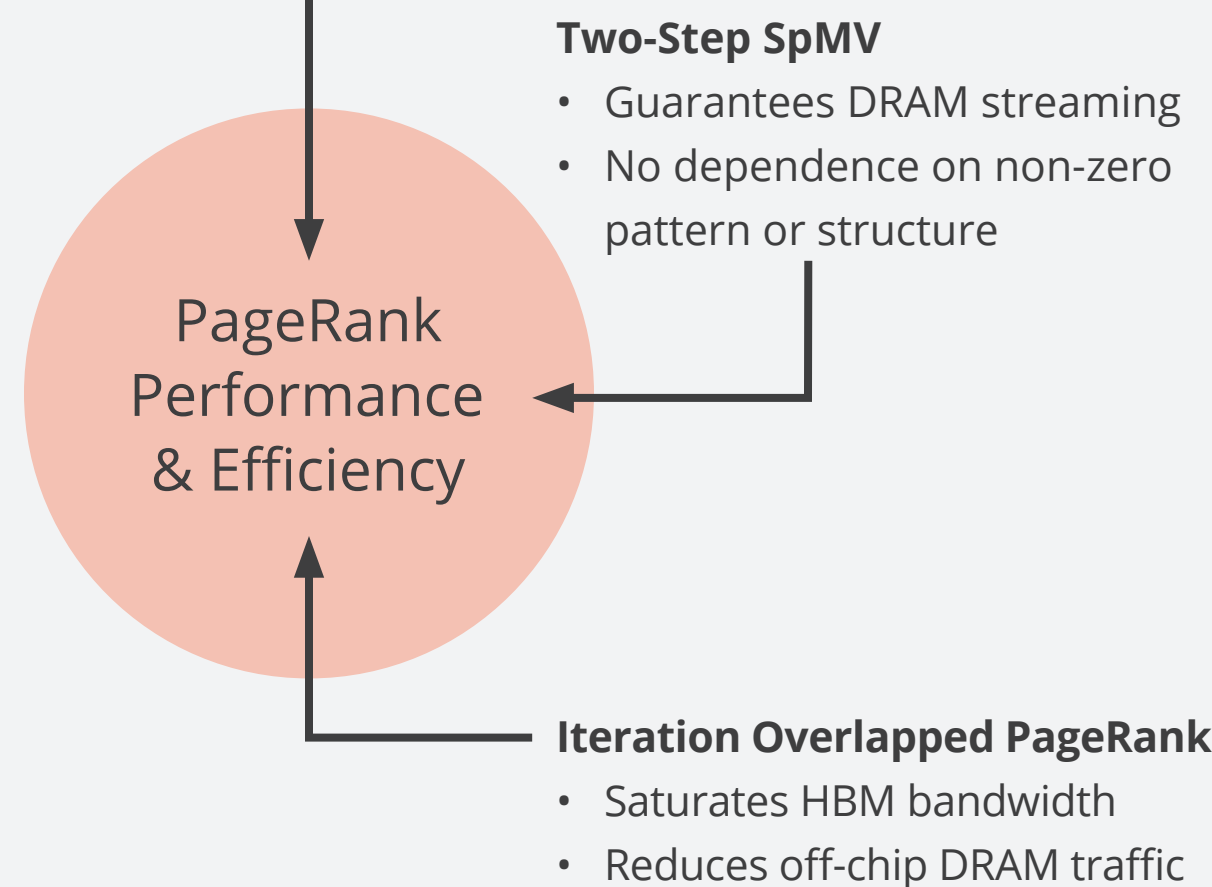


- Guarantees full DRAM streaming access
- Reduces off-chip traffic and enables high-bandwidth utilization
- **Requires custom hardware for efficient multi-way merge**

Proposed Solution

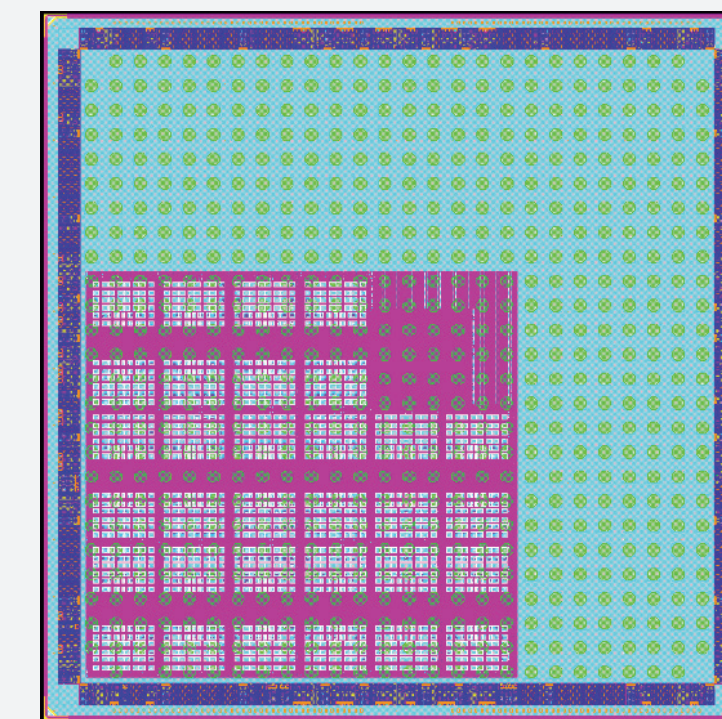
Custom Hardware with 3D HBM

- Efficient SpMV implementation
- Scalable—less fast memory required



16nm FinFET ASIC for PageRank

(can also be realized in COTS FPGA)

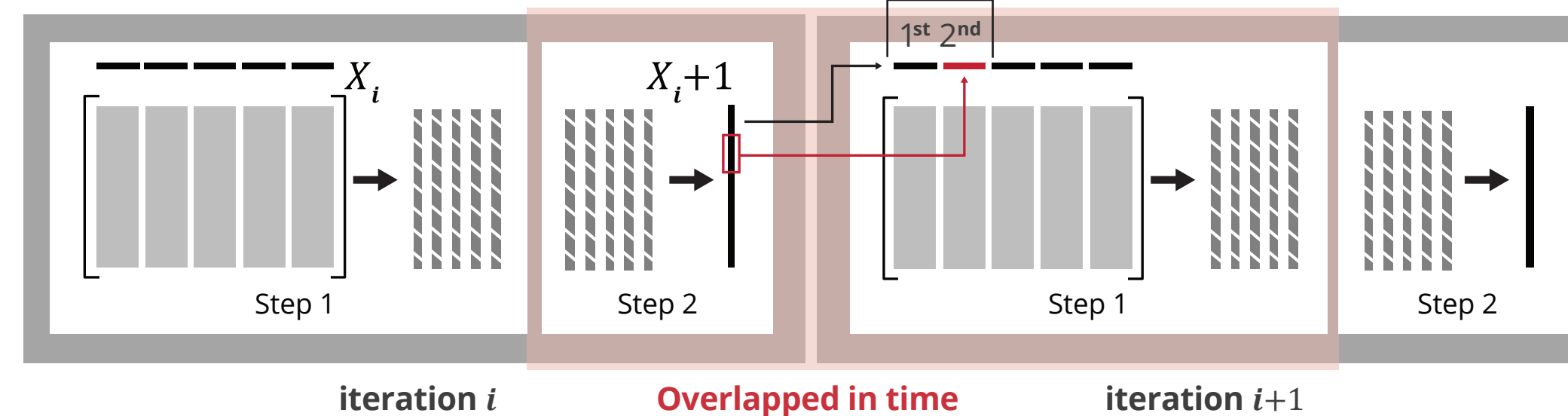


Freq.: 1.4 GHz
Area: 7.5 mm²
Power: 3.11 W

Optimized PageRank by Iteration Overlap (PR_TS_Opt)

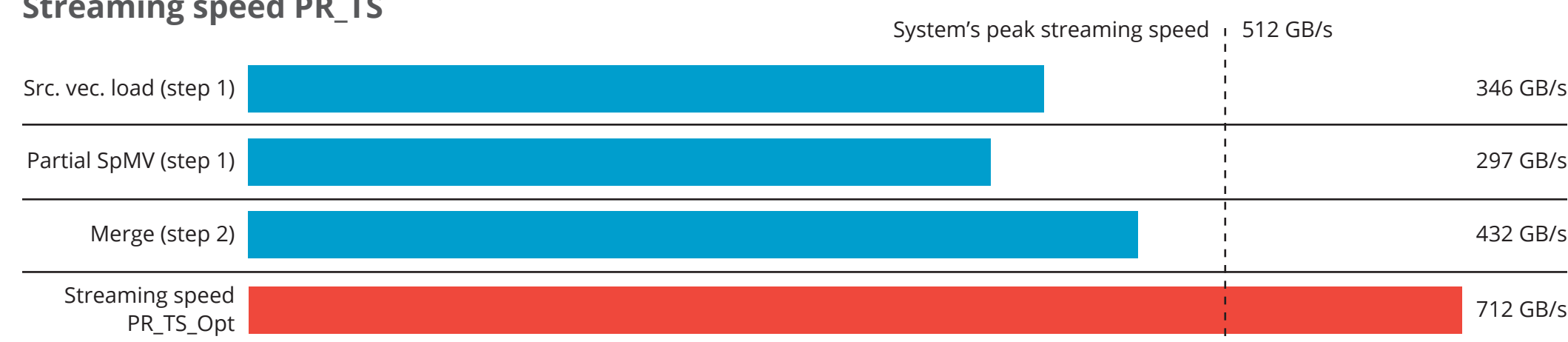
Two source vector segment storages in fast memory are required:

- 1) for computation of Step1 in iteration $i+1$ and 2) for storing output of Step 2 in iteration i .



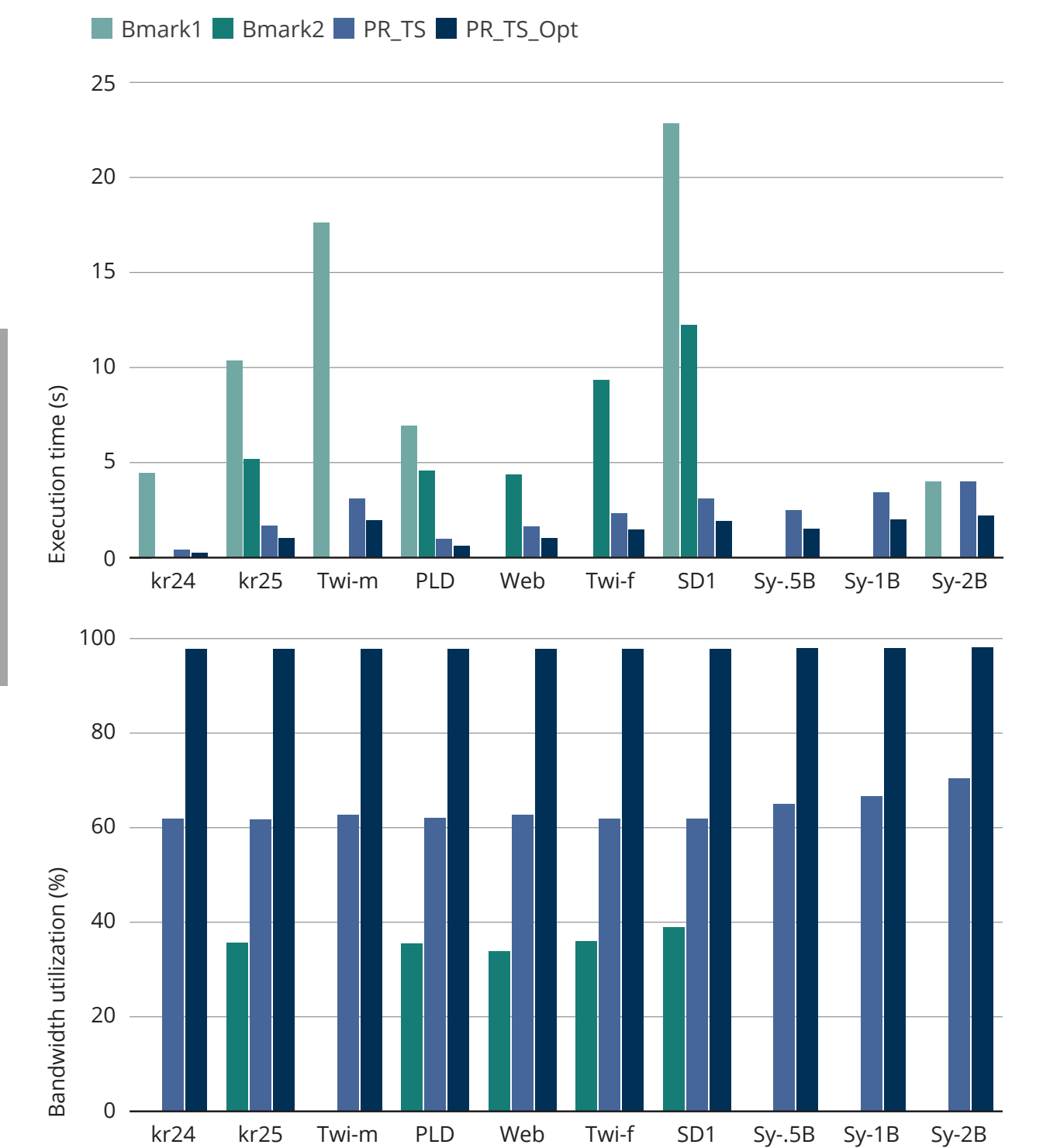
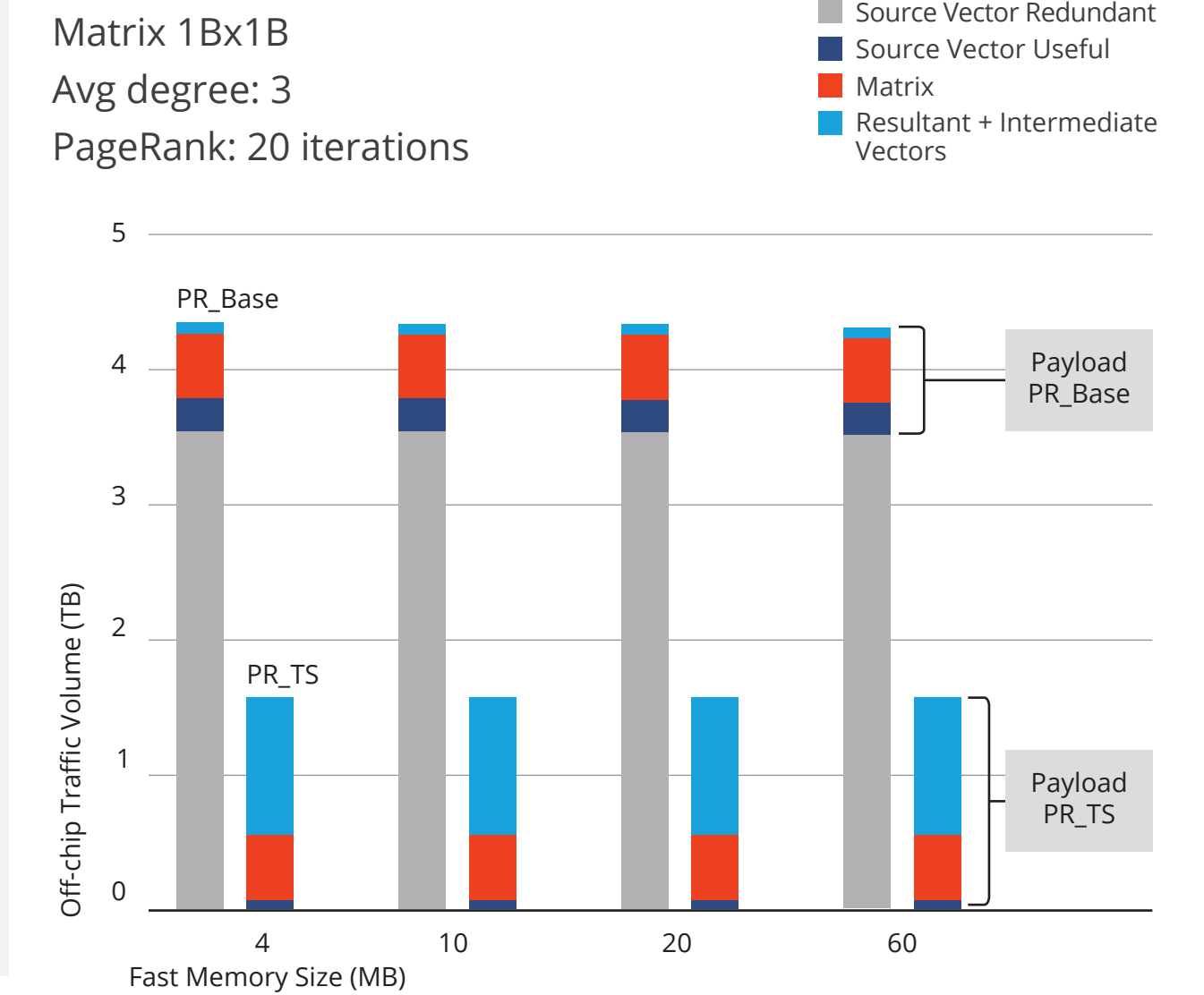
- Step 2 of an iteration runs simultaneously with Step 1 of the next iteration
- Reduces off-chip traffic by eliminating DRAM round trip of both vectors
- **Simultaneous Step 1 & 2 doubles the throughput and saturates HBM**

Streaming speed PR_TS



Experimental Results

PageRank Off-chip Traffic Comparison: PR_TS vs Baseline



Reference: F. Sadi, J. Sweeney, S. McMillan, T. Z. Low, J. C. Hoe, L. Pileggi, and F. Franchetti, "PageRank Acceleration for Large Graphs with Scalable Hardware and Two-Step SpMV," at *IEEE High Performance Extreme Computing Conference*, Waltham, MA, September 2018.

Copyright 2018 Carnegie Mellon University. All Rights Reserved.

This material is based upon work funded and supported by the Department of Defense under Contract No. FA8702-15-D-0002 with Carnegie Mellon University for the operation of the Software Engineering Institute, a federally funded research and development center.

The view, opinions, and/or findings contained in this material are those of the author(s) and should not be construed as an official Government position, policy, or decision, unless designated by other documentation.

NO WARRANTY. THIS CARNEGIE MELLON UNIVERSITY AND SOFTWARE ENGINEERING INSTITUTE MATERIAL IS FURNISHED ON AN "AS-IS" BASIS. CARNEGIE MELLON UNIVERSITY MAKES NO WARRANTIES OF ANY KIND, EITHER EXPRESSED OR IMPLIED, AS TO ANY MATTER INCLUDING, BUT NOT LIMITED TO, WARRANTY OF FITNESS FOR PURPOSE OR MERCHANTABILITY, EXCLUSIVITY, OR RESULTS OBTAINED FROM USE OF THE MATERIAL. CARNEGIE MELLON UNIVERSITY DOES NOT MAKE ANY WARRANTY OF ANY KIND WITH RESPECT TO FREEDOM FROM PATENT, TRADEMARK, OR COPYRIGHT INFRINGEMENT.

[DISTRIBUTION STATEMENT A] This material has been approved for public release and unlimited distribution. Please see Copyright notice for non-US Government use and distribution.

Internal use:* Permission to reproduce this material and to prepare derivative works from this material for internal use is granted, provided the copyright and "No Warranty" statements are included with all reproductions and derivative works.

External use:* This material may be reproduced in its entirety, without modification, and freely distributed in written or electronic form without requesting formal permission. Permission is required for any other external and/or commercial use. Requests for permission should be directed to the Software Engineering Institute at permission@sei.cmu.edu.

* These restrictions do not apply to U.S. government entities.

Carnegie Mellon® is registered in the U.S. Patent and Trademark Office by Carnegie Mellon University.

DM18-1138