Research Problem

PageRank suffers from poor performance and efficiency due to notorious memory access behavior. More importantly, when graphs become bigger and sparser, PageRank applications are inhibited as most solutions strongly rely on large random access fast memory, which is not scalable.

PageRank vector:

\[
x_i = \alpha x_i^T A + (1 - \alpha) x_i^T e^T \frac{e}{N}
\]

Target Graphs

- Very large (~billion nodes)
- Highly sparse (average degree<10)
- No exploitable non-zero pattern

Proposed Solution

Custom Hardware with 3D HBM

- Efficient SpMV implementation
- Scalable—less fast memory required

16nm FinFET ASIC for PageRank
(can also be realized in COTS FPGA)

- Guarantees DRAM streaming
- No dependence on non-zero pattern or structure

Experimental Results

PageRank Off-chip Traffic Comparison: PR_TS vs Baseline

Matrix 1Bx1B
Avg degree: 3
PageRank: 20 iterations

Step 2 of an iteration runs simultaneously with Step 1 of the next iteration
- Reduces off-chip traffic by eliminating DRAM round trip of both vectors
- Simultaneous Step 1 & 2 doubles the throughput and saturates HBM

Two-Step SpMV Algorithm

Baseline SpMV: 80M nodes, Avg. degree 3

- Traffic (Required): 37%
- Traffic (Redundant): 63%
- Pages Opened (Required): 16%
- Pages Opened (Redundant): 94%

Two-step algorithm conducts SpMV in two separate steps. It requires blocking of the matrix and the source vector as shown below.

- Guarantees full DRAM streaming access
- Reduces off-chip traffic and enables high-bandwidth utilization
- Requires custom hardware for efficient multi-way merge

Optimized PageRank by Iteration Overlap (PR_TS_Opt)

Two source vector segment storages in fast memory are required:
1) for computation of Step1 in iteration \(i + 1\) and 2) for storing output of Step 2 in iteration \(i\).

- Step 2 of an iteration runs simultaneously with Step 1 of the next iteration
- Reduces off-chip traffic by eliminating DRAM round trip of both vectors
- Simultaneous Step 1 & 2 doubles the throughput and saturates HBM

Streaming speed PR_TS

- Src. vec. load (step 1): 512 GB/s
- Partial SpMV (step 1): 546 GB/s
- Merge (step 2): 402 GB/s
- PR_TS_Opt: 712 GB/s
